Semnan University

بسم الله الرحمن الرحیم

Semnan University

Advanced Computer Architecture

Vector Computers

Teacher

Fatemeh Daraee

f_daraei@semnan.ac.ir

https://fdaraei.profile.semnan.ac.ir

Semnan University

VECTOR PROCESSOR

- Vector processors are special purpose computers that match a range of (scientific) computing tasks.

- vector processors provide vector instructions. These instructions operate in a pipeline .

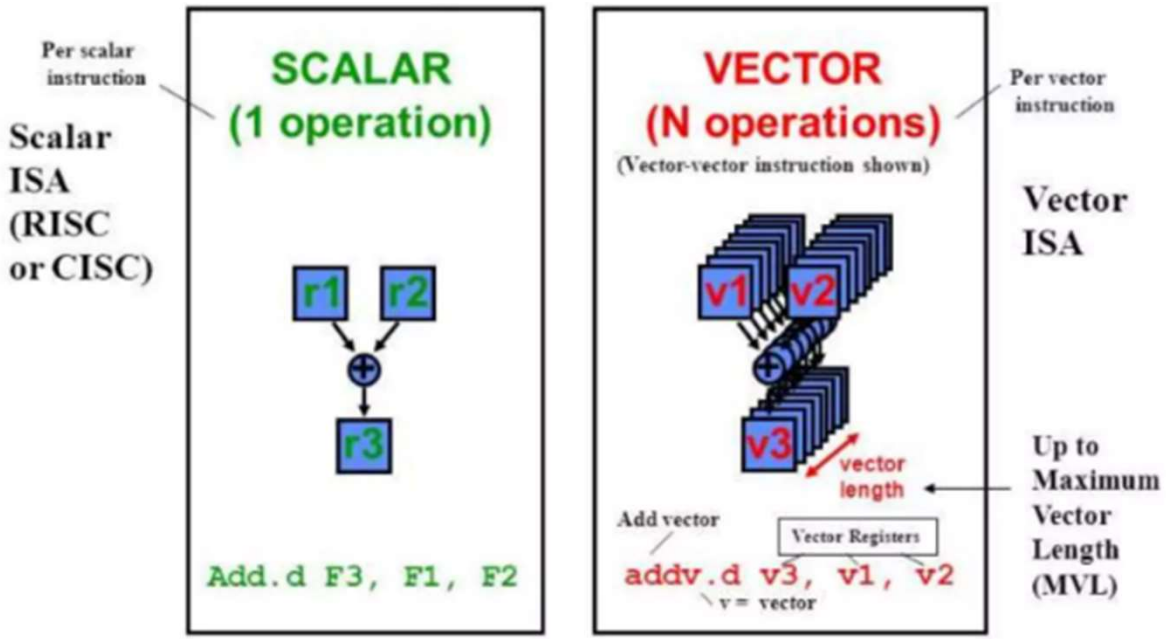
Semnan University

OBJECTIVE

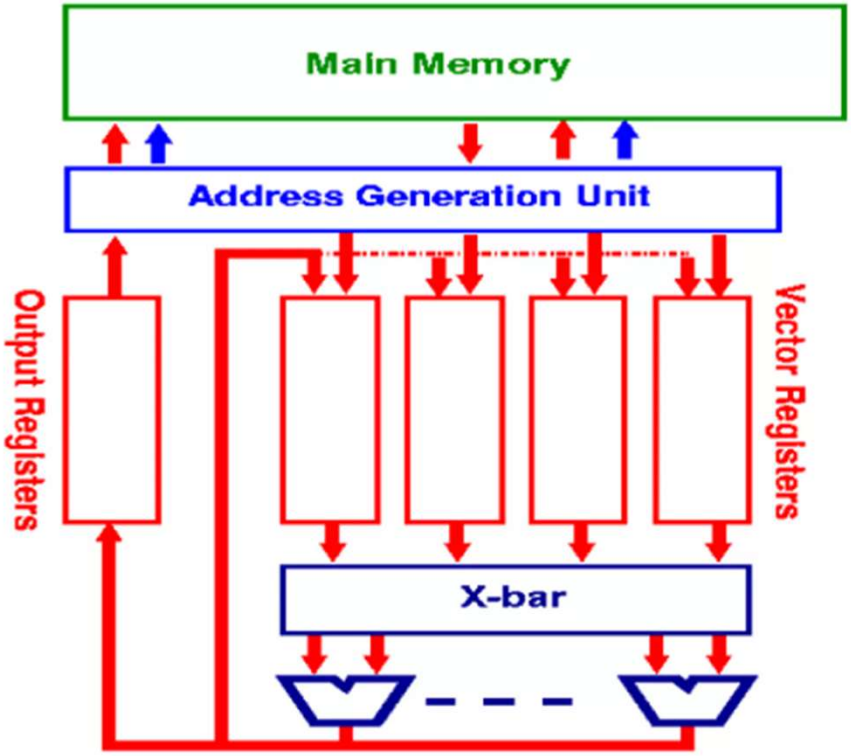
- Small Programs size
- No wastage
- Feeding of functional unit(FU) and the register buses

Semnan University

HOW IT WORKS?



HOW IT WORKS?


Main Memory
Address Generation Unit
Output Registers
Vector Registers
X-bar

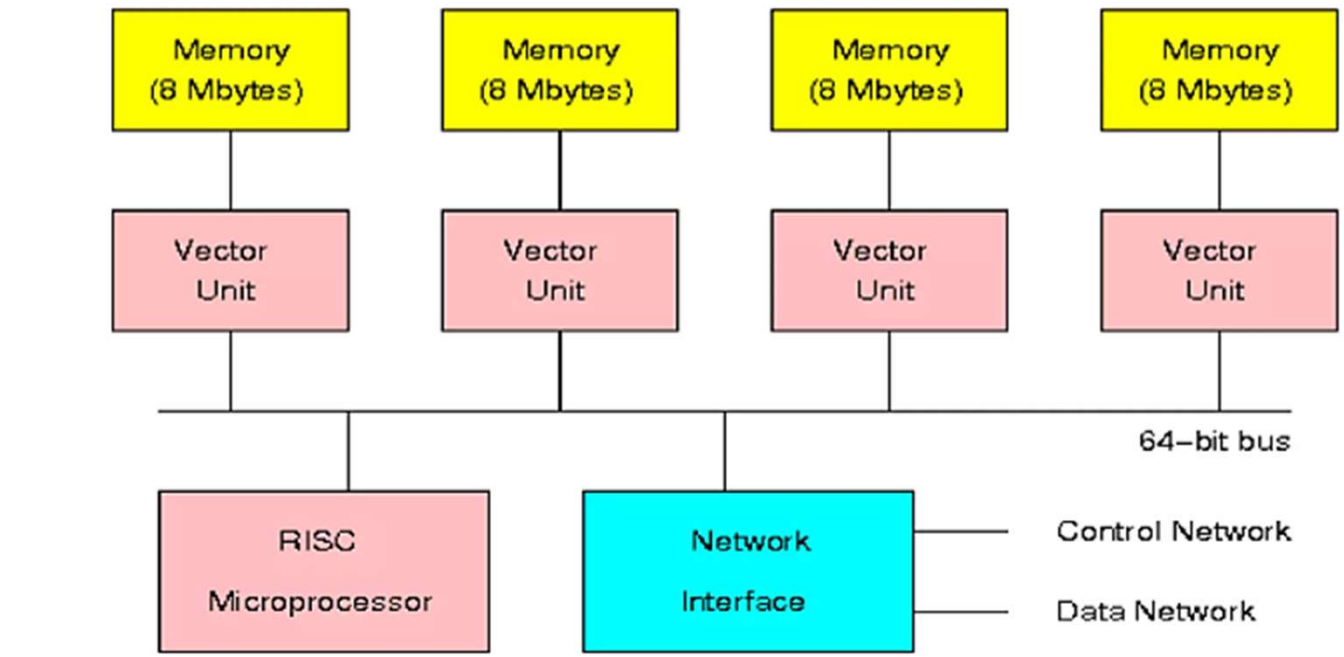
Semnan University

OPERATIONS

- Add two vectors to produce a third.
- Subtract two vectors to produce a third
- Multiply two vectors to produce a third
- Divide two vectors to produce a third
- Load a vector from memory
- Store a vector to memory.

Semnan University

ARCHITECTURE



PROPERTIES

- Vector processors reduce the fetch and decode bandwidth as the number of instructions fetched are less.
- They also exploit data parallelism in large scientific and multimedia applications.
- Many performance optimization schemes are used in vector processors.
- Strip mining is used to generate code so that vector operation is possible for vector operands whose size is less than or greater than the size of vector registers.

PROPERTIES

- Vector chaining the equivalent of forwarding in vector processors - is used in case of data dependency among vector instructions.
- Special scatter and gather instructions are provided to efficiently operate on sparse matrices.
- Instruction are designed with the property that all vector arithmetic instructions only allow element N of one vector register to take part in operations with element N from other vector registers.

PROPERTIES

- Based on how the operands are fetched, vector processors can be divided into two categories - in memory-memory architecture operands are directly streamed to the functional units from the memory and results are written back to memory as the vector operation proceeds. In vector-register architecture, operands are read into vector registers from which they are fed to the functional units and results of operations are written to vector registers.

Semnan University

ADVANTAGES

- Data can be represented at its original resolution and form without generalization.
- Accurate location of data is maintained.
- Efficient encoding of topology, and as a result more efficient operations.
- Mature, developed compiler technology
- Compact: Describe N operations with 1 short instruction

Semnan University

SOME VECTOR PROCESSORS

PROCESSOR	YEAR	CLOCK(MHZ)	REGISTER ELEMENT	FUCTIONAL (PER REGISTER)	UNITS
CRAY-1	1976	80	8	64	6
CRAY-XMP	1983	120	8	64	8
CRAY-YMP	1988	166	8	64	8
NEC SX/2	1984	160	8+8192	256 variable	16
CRAY C-90	1991	240	8	128	8
NEC SX/4	1995	400	8+8192	256 variable	16
CRAY J-90	1995	100	8	64	8
CRAY T-90	1996	500	8	128	8
NEC SX/5	1999				

NEW TERMS FOR VECTOR PROCESSORS

- Initiation rate
  - ✓consuming operands
  - ✓producing new results.
- Chime
  - ✓timing measure
  - ✓vector sequence
  - ✓ignores the startup overhead for a vector operation.

Semnan University

NEW TERMS FOR VECTOR PROCESSORS

- Convoy
  - ✓is the set of vector instructions
  - ✓potentially begin execution together in one clock period.
  - ✓must complete before new instructions can begin.

- vector start-up time
  - ✓overhead to start execution
  - ✓related to the pipeline depth

Semnan University

PROPOSED VECTOR PROCESSOR

- CODE (Clustered Organization for Decoupled Execution) is a proposed vector architecture which will overcome the some limitations of conventional vector processors.

REASONS

- Complexity of central vector register files(VRF) - In a processor with N vector functional units(VFU), the register file needs approximately 3N access ports. VRF area, power consumption and latency are proportional to O(N*N), O(log N) and O(N) respectively.
- Difficult to implement precise implementation - In order to implement in-order commit, a large ROB is needed with at least one vector register per VFU.

Semnan University

REASONS

- In order to support virtual memory, large TLB is needed so that TLB has enough entries to translate all virtual addresses generated by a vector instruction.
- Vector processors need expensive on-chip memory for low latency.

SOME FEATURES OF CODE

- Vector registers are organized in the form of clusters in CODE architecture.
- CODE can hide communication latency by forcing the output interface to look ahead into the instruction queue and start executing register move instructions.
- CODE supports precise exception using a history buffer.
- In order to reduce the size of TLB.
- CODE proposes an ISA level change.

Semnan University

The Effect of cache design into vector computers

- Numerical programs
  - ✓ data sets that are too large for the current cache sizes.
  - ✓Sweep accesses of a large vector
  - ✓result in complete reloading of the cache
- achieve high memory bandwidth
  - ✓Register files
  - ✓highly interleaved memories
- Address sequentiation

Proposals of cache schemes

- Proposals such as prime-mapped cache schemes have been proposed and studied. The new cache organization minimizes cache misses caused by cache line interferences that have been shown to be critical in numerical applications.
- The cache lookup time of the new mapping scheme keeps the same as conventional caches. Generation of cache addresses for accessing the prime-mapped cache can be done in parallel with normal address calculations.

Conclusion

- Vector supercomputers
- Vector instruction
- Commodity technology like SMT
- Superscalar microprocessor
- Embedded and multimedia applications

Semnan University

Vector Supercomputers

Epitomized by Cray-1, 1976:

- Scalar Unit
  - Load/Store Architecture
- Vector Extension
  - Vector Registers
  - Vector Instructions
- Implementation
  - Hardwired Control
  - Highly Pipelined Functional Units
  - Interleaved Memory System
  - No Data Caches
  - No Virtual Memory